

REMARKS

Claims 1, 2, 17 and 25 have been amended to place them in proper form for allowance.

In response to the Advisory Action of July 16, 2002, it is again requested that U.S. Serial No. 09/432,662 be indicated as being considered by the Examiner before issuance of the above-identified application.

It is noted the applicants' previous response submitted May 29, 2002, there is no requirement that the identified related application include pending allowed claims. 37 C.F.R. 1.56 places a burden on the applicant to disclose to the U.S. Patent and Trademark Office information material to patentability. Further, it requires that this information be submitted to the Office in the manner described by 37 C.F.R. 1.97(b)-(d) and 1.98. In accordance with 37 C.F.R. 1.98, applicant in the Information Disclosure Statement filed November 30, 2001 included for each cited pending U.S. application, the application specification including the claims, and any drawings of the application. As the Examiner can fully appreciate, there is no requirement for consideration of a related application that one or more claims of the related application be indicated as being allowable.

Applicant is under a duty to disclose information related to the patentability of the present application and consequently it is respectfully submitted that applicant has fulfilled this duty in presentation of the information set forth in the Information Disclosure Statement filed November 30, 2001 and it is respectfully requested that the Examiner properly indicate consideration of such application by properly initialing the Form PTO-1449 which accompanied such Information Disclosure Statement. It is unclear why the Examiner believes that there is any requirement that patent applications disclosed to the U.S. Patent and Trademark Office under applicants' duty of disclosure set forth in 37 C.F.R. 1.56 which are filed in compliance with 37 C.F.R. 1.98 require an indication that there are allowed claims pertinent to this invention set forth in the related applications. While such allowed

claims may be relevant to the issue of double patenting, there is no such requirement for the Examiner to indicate consideration of the subject matter set forth in the related applications. Accordingly, in that the U.S. Patent and Trademark Office has placed this burden on the applicant, it is only fitting that the Examiner indicate his consideration of the related applications submitted in accordance therewith. Such applications include U.S. Application Serial Nos. 09/432,662; 09/580,485 and 09/587,369 as identified in applicants' Form PTO-1449 filed November 30, 2001. Should the Examiner maintain his position in this regard, he is hereby requested to provide support for such position.

Examination on the merits is requested.

Respectfully submitted,



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VERSION WITH MARKINGS TO SHOW CHANGES MADE

1. (Twice Amended) An electroluminescence display device [which comprises a pixel] comprising:

a substrate; [and]

a plurality of pixels over the substrate, each of the plurality of pixels comprising:

a first thin film transistor;

a second thin film transistor comprising a gate electrode electrically connected to the first thin film transistor; and

an electroluminescence element electrically connected to the second thin film transistor,

wherein the first thin film transistor comprises [an active layer in which 2 or greater number of channel regions connected in series are formed.] at least two channel regions in an active layer, at least two gate electrodes corresponding to the channel regions, over the active layer with a gate insulating film interposed therebetween, and an impurity region interposed between the channel regions.

2. (Twice Amended) An electroluminescence display device comprising:

a substrate; and

a plurality of pixels over the substrate, each of the plurality of pixels comprising:

a first thin film transistor;

a second thin film transistor comprising a gate electrode electrically connected to the first thin film transistor; and

an electroluminescence element electrically connected to the second thin film transistor,

wherein the first thin film transistor comprises [an active layer in which 2 or greater number of channel regions connected in series are formed,] at

least two channel regions in an active layer, at least two gate electrodes corresponding to the channel regions, over the active layer with a gate insulating film interposed therebetween, and an impurity region interposed between the channel regions, and

wherein a channel width of the second thin film transistor is greater than a channel width of the first thin film transistor.

17. (Amended) An electroluminescence display device comprising:

a substrate; and

a plurality of pixels over the substrate, each of the plurality of pixels comprising:

a first thin film transistor;

a second thin film transistor comprising a gate electrode electrically connected to the first thin film transistor; and

an electroluminescence element electrically connected to the second thin film transistor,

wherein the first thin film transistor comprises [an active layer in which at least two channel regions connected in series are formed with an impurity region interposed therebetween.] at least two gate electrodes over the substrate, at least two channel regions corresponding to the gate electrode, over the gate electrode with a gate insulating film interposed therebetween, and an impurity region interposed between the channel regions.

25. (Amended) An electroluminescence display device comprising:

a substrate; and

a plurality of pixels over the substrate, each of the plurality of pixels comprising:

a first thin film transistor;

a second thin film transistor comprising a gate electrode electrically connected to the first thin film transistor; and

an electroluminescence element electrically connected to the second thin film transistor,

wherein the first thin film transistor comprises [an active layer in which at least two channel regions connected in series are formed with an impurity region interposed therebetween,] at least two gate electrodes over the substrate, at least two channel regions corresponding to the gate electrode, over the gate electrode with a gate insulating film interposed therebetween, and an impurity region interposed between the channel regions, and

wherein a channel width of the second thin film transistor is greater than a channel width of the first thin film transistor.